CLAIMS

What is claimed is:

1. A method for energy and power estimation of a core-model based embedded system, the method including:

capturing gate-level energy simulation data;

deploying the captured gate-level simulation data in an algorithmic-level executable specification, wherein the captured gate-level data simulation data correlates to a plurality of instructions; and

executing the algorithmic-level executable specification to obtain energy estimations for each instruction;

2. A method of modeling energy and power requirements for a system-on-a-chip, the modeling method including:

deploying a circuit model of the system-on-a-chip by selecting at least one parameterized instruction-based core model and instantiating the at least one parameterized instruction-based core model;

executing the circuit model;

analyzing the estimated energy requirements of the circuit model; and

outputting the estimated energy requirements for the circuit model.

3. The method of modeling energy and power requirements for a system-on-a-chip as claimed in claim 2, wherein the least one parameterized instruction-based core model includes toggle counts for a plurality of implementations of the deployed circuit model.

4. A method for creating a library of instruction-based core

energy models, the method including:

deploying a circuit model using a hardware description language;

defining a plurality of high-level instructions correlating to functions supported by the circuit model;

acquiring gate-level energy simulation data for each component comprising the circuit model;

collecting a plurality of toggle count sets corresponding to each of the plurality of high-level instructions;

assigning each of the plurality of toggle count sets to one of the plurality of high-level instructions, thereby creating an instruction-based core energy model; and

implementing the instruction-based core energy model within the library that is realized as a look-up table.

5. The method for creating a library of instruction-based core energy models as claimed in claim 4, wherein the step of assigning each of the plurality of toggle count sets to one of the plurality of instructions further includes increasing the number of high-level instructions to reduce data dependency.

6. A computer program product for use in a computer system in which core models are accessed by an application program, the computer program product including a computer usable medium bearing computer executable code, the computer executable code including:

a first executable code portion for determining if the core model should simulate an idle state or execute an instruction, based upon whether the core model is called by another core model or it is called by a

control object;

a second executable code portion for determining if resources required by the core model are free, and claiming the free resources;

a third executable code portion for adding an idle energy value to an energy accumulator;

a fourth executable code portion for determining if a clock counter are decremented, thereby collecting data about the elapsed time and calculating the consumed power from the energy data;

a fifth executable code portion for simulating execution of a predetermined instruction; and

a sixth executable code portion for adding energy value to the energy accumulator;

7. A computer program product for use in a computer system in which core models are accessed by an application program, the computer program product including:

a computer usable medium bearing computer programming statements for enabling the computer system to create at least one circuit model object for use by the application program;

the computer programming statements including a class library expressing an inheritance hierarchy and including at least one core model base class for constructing instances of the at least one circuit model object, the core model base class representative of a circuit element;

the at least one core model base class including, as a respective subclass thereof, an autonomous core model class defining at least one core model member function for directly interacting with the application

program; and

the at least one core model member function simulating an instruction associated to the circuit element, the circuit element providing one-time predetermined data correlated to the simulated instruction.

8. In a computer system having an application program that models the energy and power requirements of a system-on-a-chip circuit design, an energy and power modeling method for an application program to access and execute a parameterized core model of a circuit element, the method including:

providing to the application program a circuit object representing a modeled circuit, the circuit object having instantiated at least one parameterized core model having at least one member function for simulating functions assigned to circuit element, wherein the at least one member function outputs an energy and power estimation correlated with each simulated function;

sending a message from the application program to the circuit object to invoke the at least one member function, thereby executing a simulated function of the circuit element; and

sending a message from the circuit object to the application program embodying the energy and power estimation with respect to the invoked member function.